# II B.Tech I Semester Regular Examinations, March-2021 DIGITAL CIRCUITS AND LOGIC DESIGN <br> (Common to ECE, CSE and IT) 

Time: 3 Hours
Max. Marks: 60
Note: Answer ONE question from each unit ( $\mathbf{5} \times \mathbf{1 2}=\mathbf{6 0}$ Marks)

## UNIT-I

1. a) Obtain X and Y from (i) and (ii), respectively
(i) (AAAA.AA) ${ }_{16}=(\mathrm{X})_{8}$
(ii) $(212212)_{3}=(Y)_{6}$
b) Let $\mathrm{A}=(11101111)_{2}$ and $\mathrm{B}=(00010001)_{2}$ are represented in 2 's complement form by using 8 -bits, perform the following operations on A and B and represent the result using 16 -bits.
(i) $\mathrm{A}+\mathrm{B}$ (ii) $\mathrm{A}-\mathrm{B}$ (iii) $\mathrm{A} * \mathrm{~B}$ (iv) $\mathrm{A} / \mathrm{B}$.
(OR)
2. Provide 16 basic distinct identities of Boolean Algebra.

## UNIT-II

3. a) Simplify the following logic function using Quine-McCluskey minimization technique.
$\mathrm{F}(\mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{D}, \mathrm{E})=\Sigma \mathrm{m}(2,4,6,8,23,25,27,29)$
b) Simplify function $\mathrm{F}(\mathrm{A}, \mathrm{B}, \mathrm{C})=\Sigma \mathrm{m}(1,2,4,7)$ and implement using NAND gates.
4. Design a full subtractor circuit. Provide truth table, K-maps, Boolean functions and logic diagrams.

## UNIT-III

5. Design an efficient 64-bit adder using full adders.

If the delay of a full adder is 2 units, then calculate delay of your design.

## (OR)

6. a) Write differences between ROM and PROM
b) Implement $\mathrm{F}(\mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{D}, \mathrm{E})=\Sigma \mathrm{m}(0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30)$ using PROM and explain its procedure?

UNIT-IV
7. a) Draw the logic diagram of a D-Latch using NAND gates. Explain its Operation using excitation table?
b) Draw and explain 4-bit bi-directional shift register
(OR)
8. a) Explain the difference between sequential and combinational circuits?
b) Design a Modulo-4 ripple counter?

## UNIT-V

9. a) Obtain the state table and state diagram for a sequence detector to recognize two consecutive zeros or ones.
b) How the Mealy is different from the Moore machine?

## (OR)

10. Derive circuit that realizes the FSM defined by the state assigned table below [12M] using JK flip flops.

| PS | $\mathrm{NS}, \mathrm{Z}$ |  |
| :---: | :---: | :---: |
|  | $\mathrm{X}=0$ | $\mathrm{X}=1$ |
| A | $\mathrm{~B}, 0$ | $\mathrm{E}, 0$ |
| B | $\mathrm{E}, 1$ | $\mathrm{D}, 0$ |
| C | $\mathrm{D}, 0$ | $\mathrm{~A}, 0$ |
| D | $\mathrm{C}, 1$ | $\mathrm{E}, 1$ |
| E | $\mathrm{B}, 0$ | $\mathrm{D}, 0$ |

